REMARKS

The Office Action of November 1, 2005 has been carefully considered. In response thereto, the claims have been amended as set forth above. Reconsideration and allowance in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 16-21 were rejected under 35 USC 112, second paragraph as being indefinite, particularly with respect to the expression "at least partially simultaneous." This expression refers to the time-overlapping transfer of two different sets of data, such that the transfers need not begin at the same time or end at the same time; however, if one transfer begins later than another, that it begins prior to the conclusion of the earlier-beginning data transfer. In this respect, the expression is believed to be clear and unambiguous. Should the Examiner wish to propose alternative phraseology, however, Applicant would be happy to consider the same.

Claims 16-21 were rejected under 35 USC 103 as being unpatentable over Whetsel in view of Nayak. The rejection states in part:

> Whetsel does not explicitly disclose that each cell of the first and the second shift register, respectively, is coupled between an external pin and one of the test arrangements. However...Nayak...discloses a method of testing an integrated circuit...including boundary scan cells 24 and 26, which are coupled with input/output pins 18 and 20 and scan elements (SEs) 25 arranged internal to the circuit 14, (Figure 1, Nayak). It would have been obvious...to implement the test architecture in the testing method of Whetsel...by sending test vectors in parallel or serial form to input pins of the integrated circuit...since parallel deliver and receipt of test vectors and test results to and from the boundary scan cells provides for ease by which the test vectors can be placed upon the scan elements arranged in one or more chains internal to the core logic. Parallel deliver and recept greatly enhances the overall test time and minimizes the test vector memory access times of the ATE....

This rejection is respectfully traversed.

Whetsel and Nayak represent opposite testing approaches. It would not have been obvious to combine the teachings of the references in a manner to arrive at the present invention.

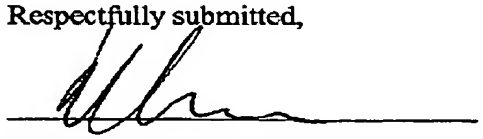
More particularly, Whetsel teaches serial input of test vectors via a single IC pin. Scan distributor and scan collector circuits are then used to provide parallel connection to multiple scan paths.

Nayak teaches parallel input of test vectors via a potentially large number of IC pins. Each test vector bit is input to a different boundary scan cell.

There is nothing in the references themselves that would teach or suggest the approach of the present invention in which test vectors are input as multiple simultaneous or partially simultaneous serial streams, which are each then converted to multiple simultaneous or partially simultaneous parallel streams.

Allowance of claims 16-21 is respectfully requested.

Respectfully submitted,



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